



Miroslav N. Velev, (www.miroslav-velev.com) mvelev@gmail.com
Aries Design Automation, USA (www.aries-da.com)

Summary

The talk will summarize results from more than two decades of exploiting efficient modeling techniques at a high level of abstraction, which combined with suitable translation to Boolean Satisfiability (SAT) allow us to formally verify complex pipelined/superscalar/VLIW microprocessors. This method is based on using the property of Positive Equality, and block-level translation to SAT. These techniques outperform other approaches for formal verification of microprocessors by orders of magnitude, while requiring minimal manual intervention, and scale for mathematically proving of both safety and liveness for a wide range of microprocessor architectures with many architectural mechanisms: branch prediction, exceptions, multicycle functional units, advanced and speculative loads, predicated execution, register remapping, out-of-order execution based on a reorder buffer, delayed branches, data-value prediction, mechanisms to correct soft errors by re-executing affected instructions, reconfigurable functional units, arrays of reconfigurable processing elements, multi-threaded execution, and reconfigurable polymorphic heterogeneous multi-core architectures. CNF formulas generated in this work 20 years ago have been used in the development of all academic and industrial SAT solvers since then.