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# FEM Modeling for PCB Assembly Simulation

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# Resume

## CURRENT POSITION/INSTITUTION

**Research Fellow, National Center for High Performance Computing (NCHC), National Applied Research Laboratories, Taiwan**

## EDUCATION

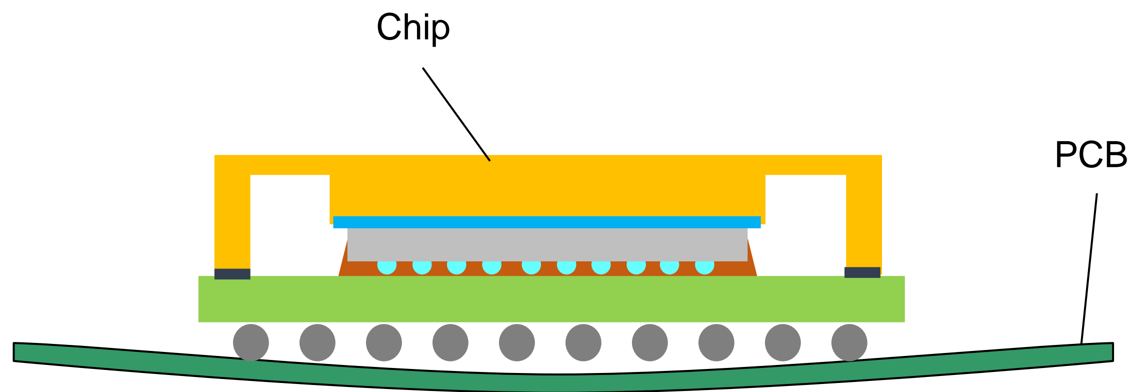
**National Tsing Hua University, Taiwan, Dept. of Mechanical Engineering, PHD.**

## RESEARCH FIELDS

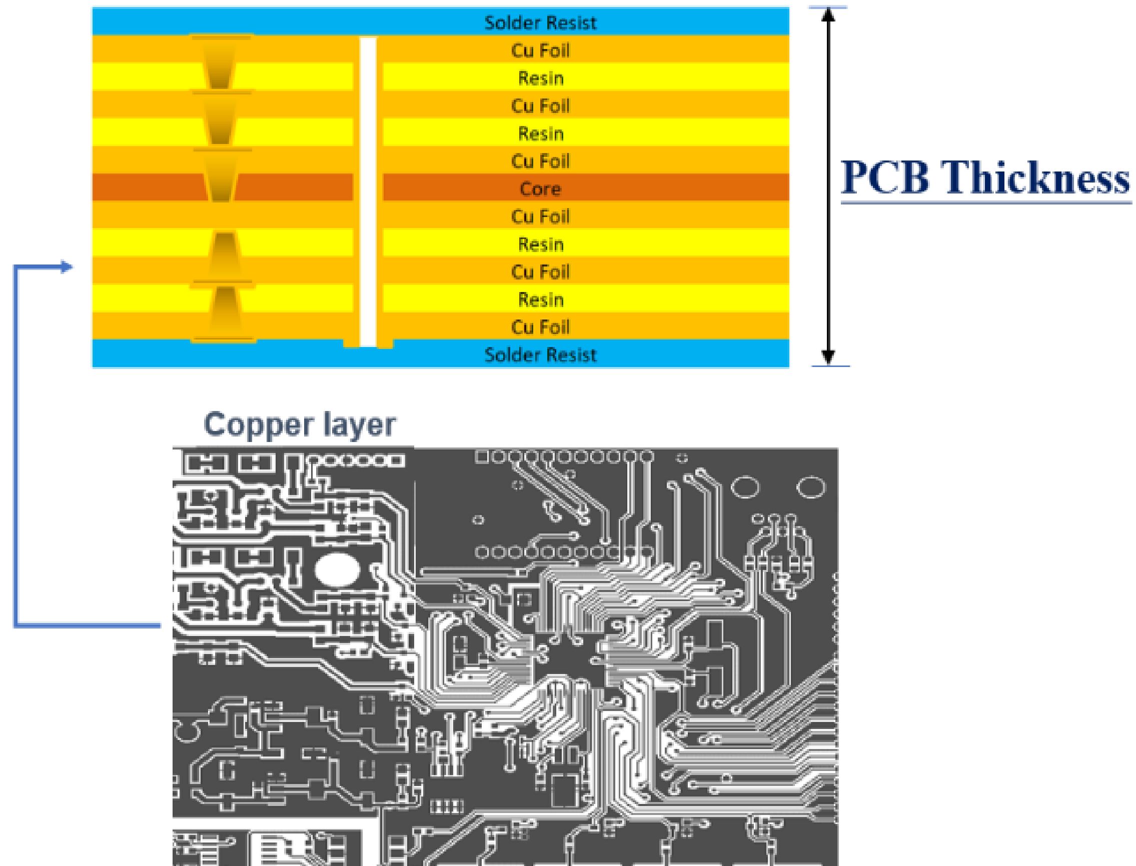
**- Solid mechanics, numerical simulation.**
**- Numerical methods, mesh generation, meshless method.**
**- 3D printing, PCBA deformation simulation, bio-mechanical simulation.**

# PCBA Warpage Problems Induced by Thermal Mismatch during Temperature Change

- Induced by the unevenly distribution of copper circuits, multi-materialled components
- Causes:
  - Solder opens
  - Stress concentration
  - Shorter fatigue life



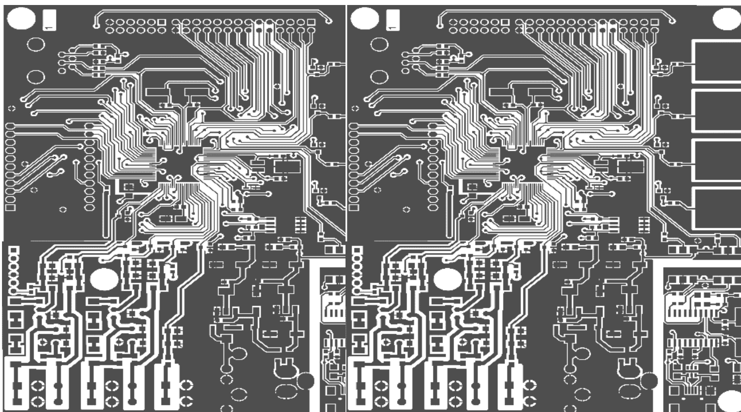
# PCB Stack-Up

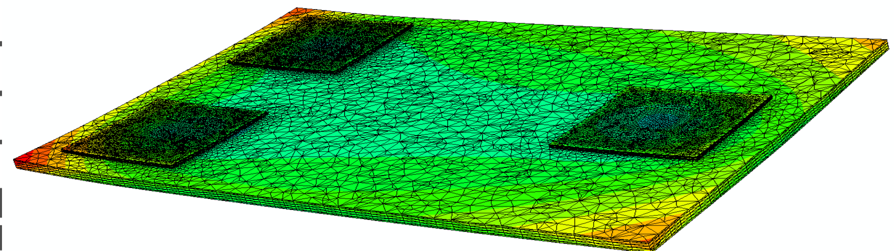


# Difficulties with Multi-scaled Problems

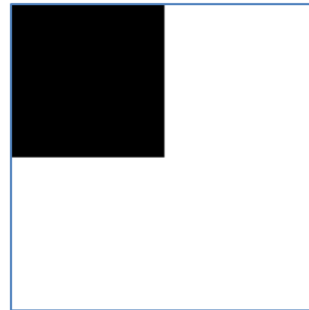
- **Circuit traces are too tiny**
  - Impossible to directly model the circuit traces
  - The scale of circuit traces is much smaller than that of PCB boards
  - Solid element models will be too big for simulation

- **Non-even distribution of circuit traces**
  - Composite material properties are different at different locations

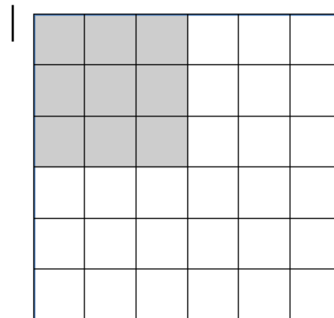




# Trace Mapping

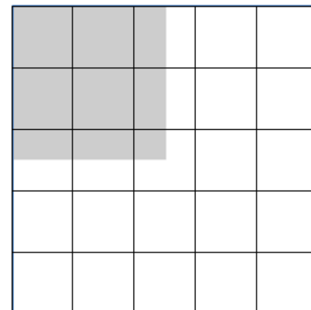


**Ratio of copper area**



(6 x 6)

| | | | | | |
|---|---|---|---|---|---|
| 1. | 1. | 1. | 0. | 0. | 0. |
| 1. | 1. | 1. | 0. | 0. | 0. |
| 1. | 1. | 1. | 0. | 0. | 0. |
| 0. | 0. | 0. | 0. | 0. | 0. |
| 0. | 0. | 0. | 0. | 0. | 0. |
| 0. | 0. | 0. | 0. | 0. | 0. |



(5 x 5)

| | | | | |
|---|---|---|---|---|
| 1. | 1. | .5 | 0. | 0. |
| 1. | 1. | .5 | 0. | 0. |
| .5 | .5 | .25 | 0. | 0. |
| 0. | 0. | 0. | 0. | 0. |
| 0. | 0. | 0. | 0. | 0. |

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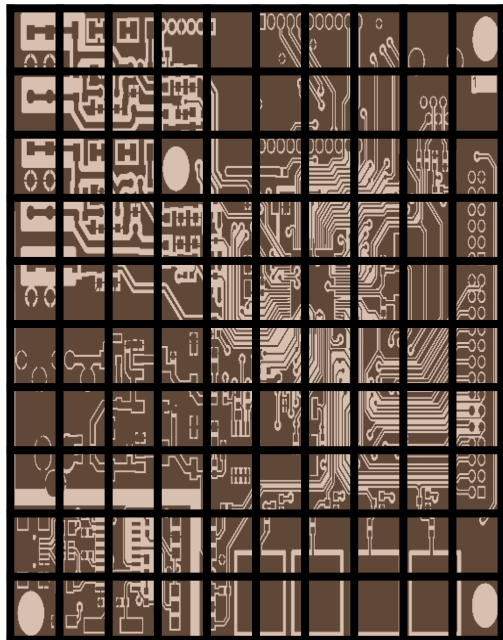
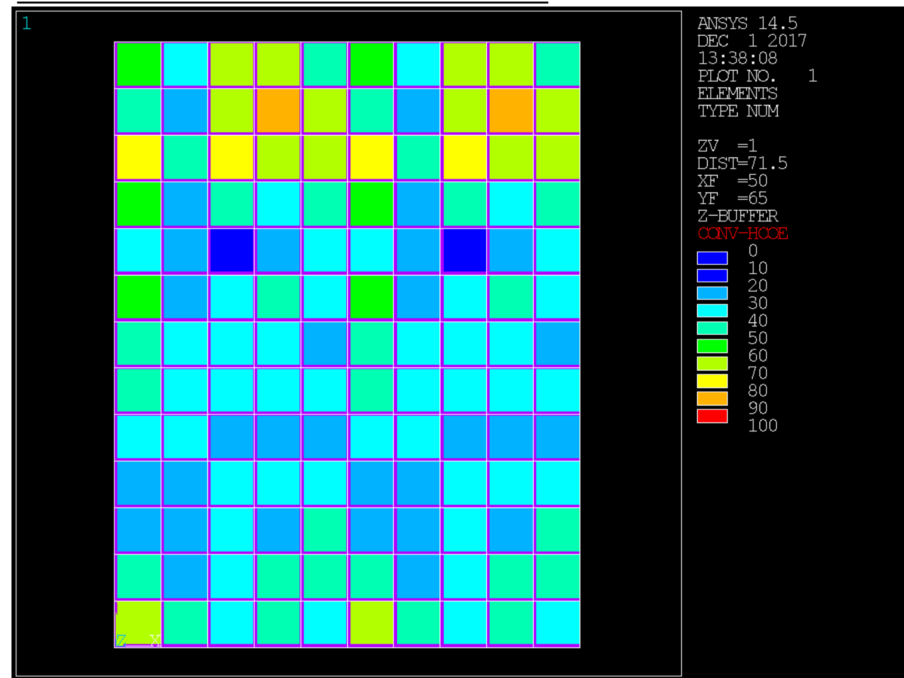
# Trace Mapping



## Area ratio of copper



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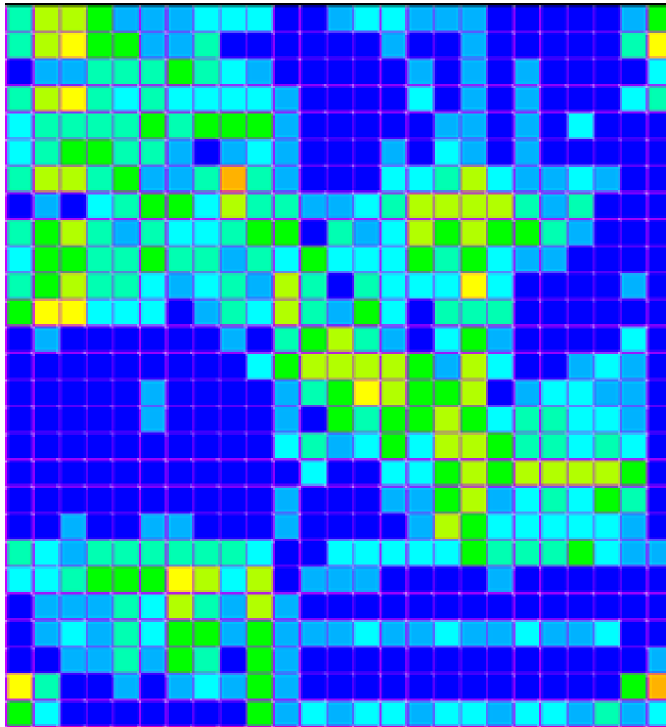
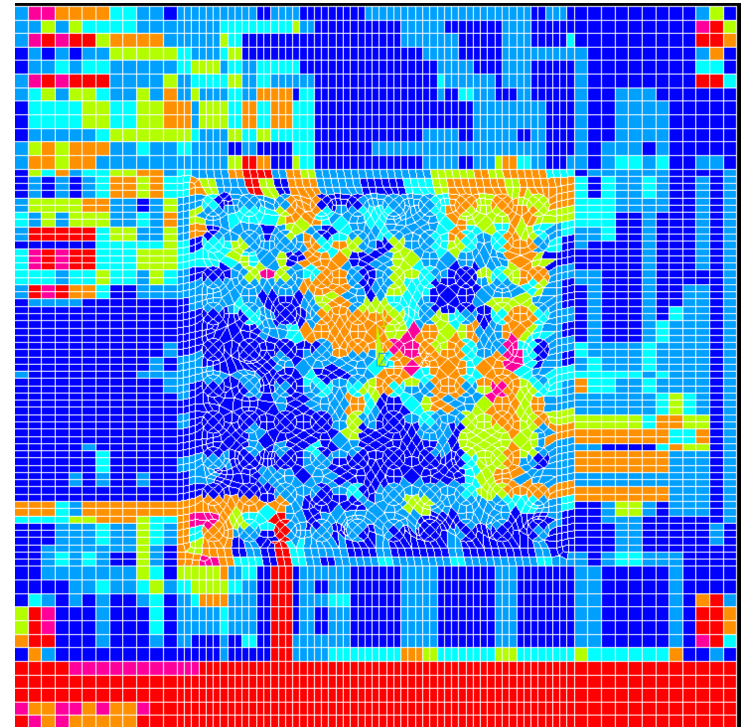
# Trace Mapping

**Area ratio of copper**



**Regular Mapping**



**Irregular Mapping**

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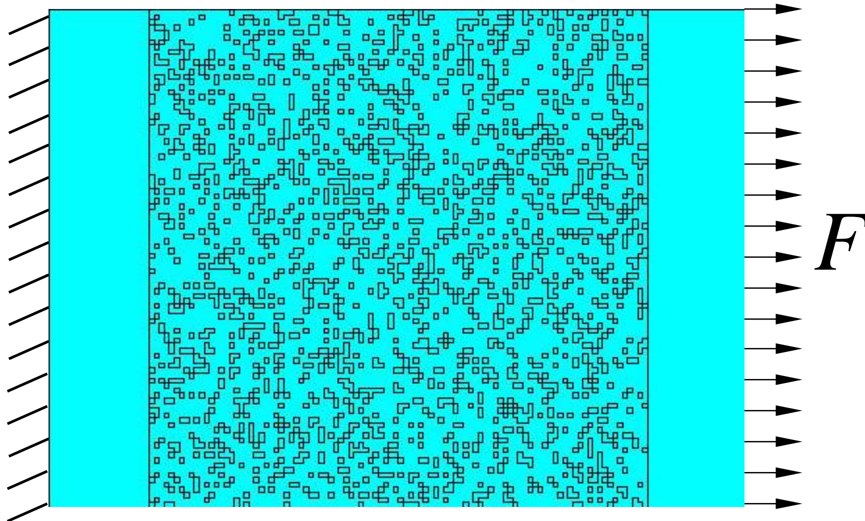
# Equivalent Young's Modulus & CTE

- Effective material property $\alpha_{IJK}$ for element **IJ** on layer **K** is then computed as:
- (1) $\alpha_{IJK} = (\delta / 100) * \alpha_{metal} + (1 - \delta / 100) * \alpha_{ep}$ for copper layers
- (2) $\alpha_{IJK} = \alpha_{dielectric}$ for dielectric layers
- Where $\alpha$ is:
  - Co-efficient of thermal expansion
  - Young's modulus of elasticity

# Equivalent Young’s Modulus

**Randomly-distributed copper**

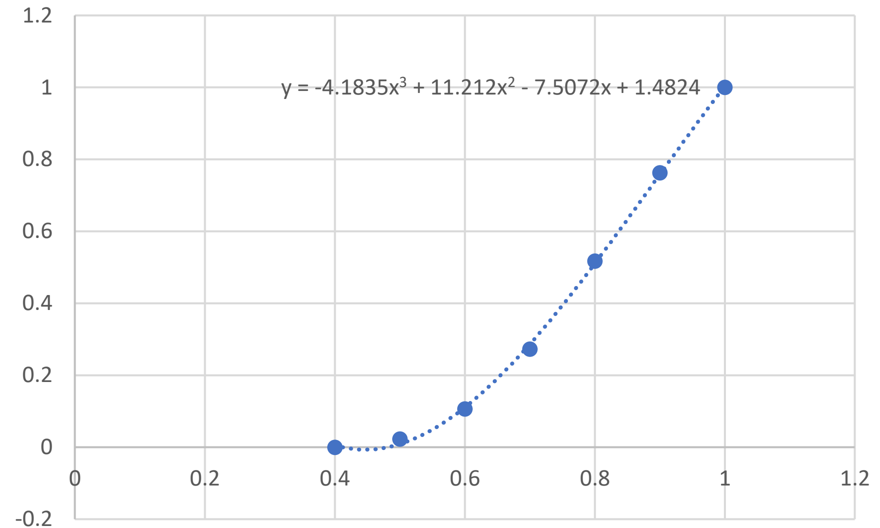



**Subjected to a tensile load**

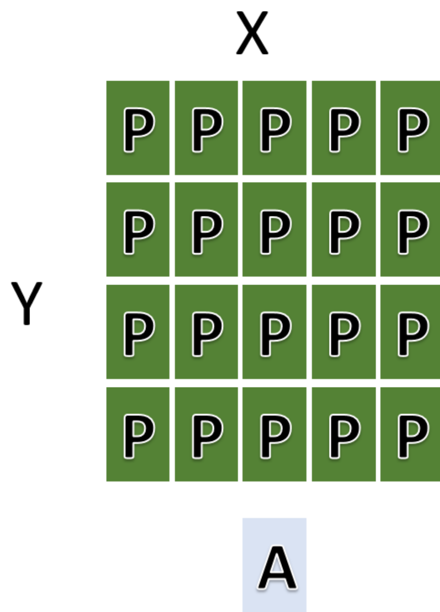
$$\sigma = E\varepsilon$$

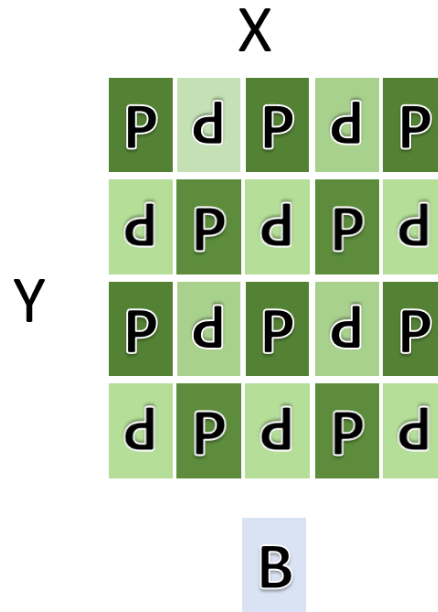
$$\frac{F}{A} = E\frac{d}{l} \quad >> \quad E = \frac{Fl}{Ad}$$

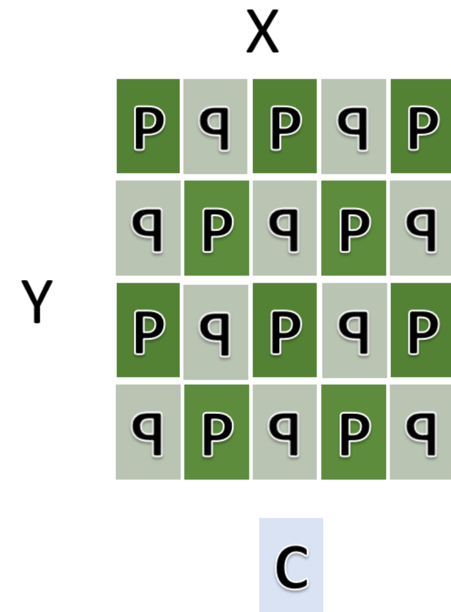
Equivalent Young’s Modulus



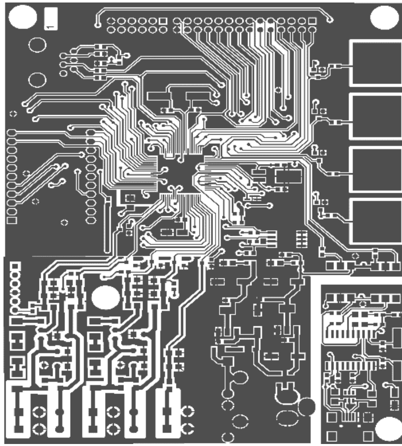
# Panel arrangement

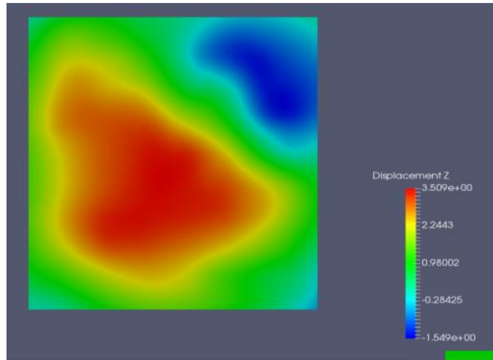


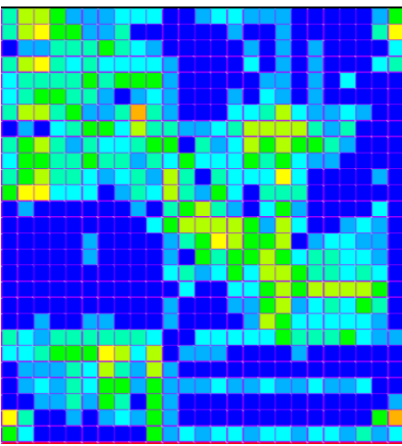



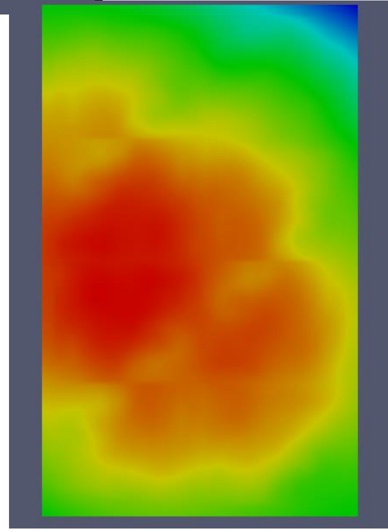



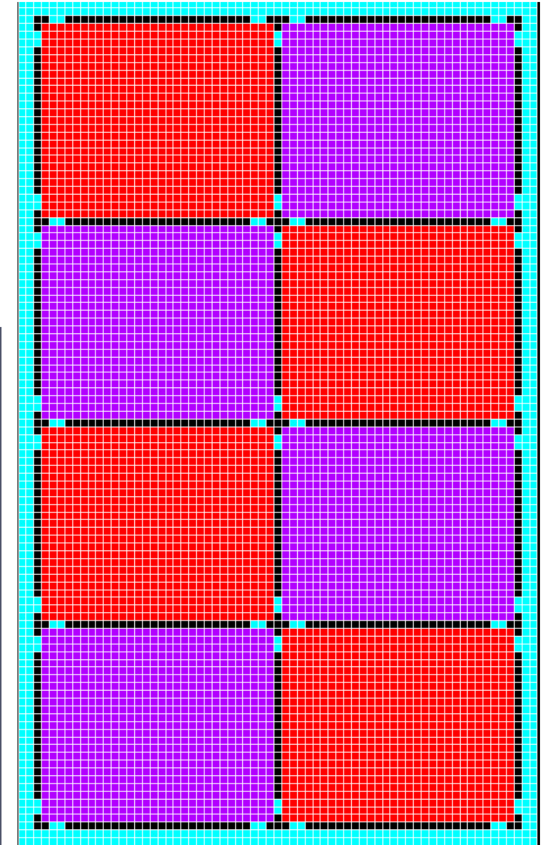
# PCB Analysis : Module & Panel



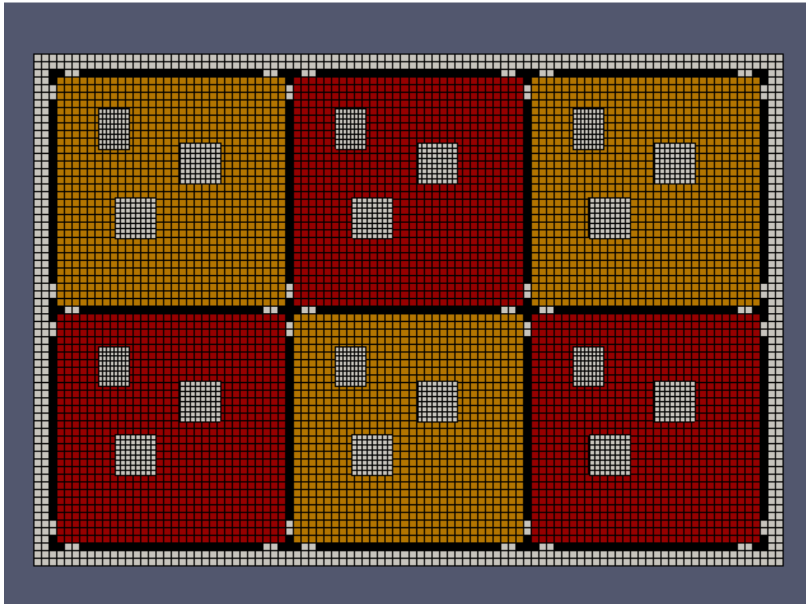


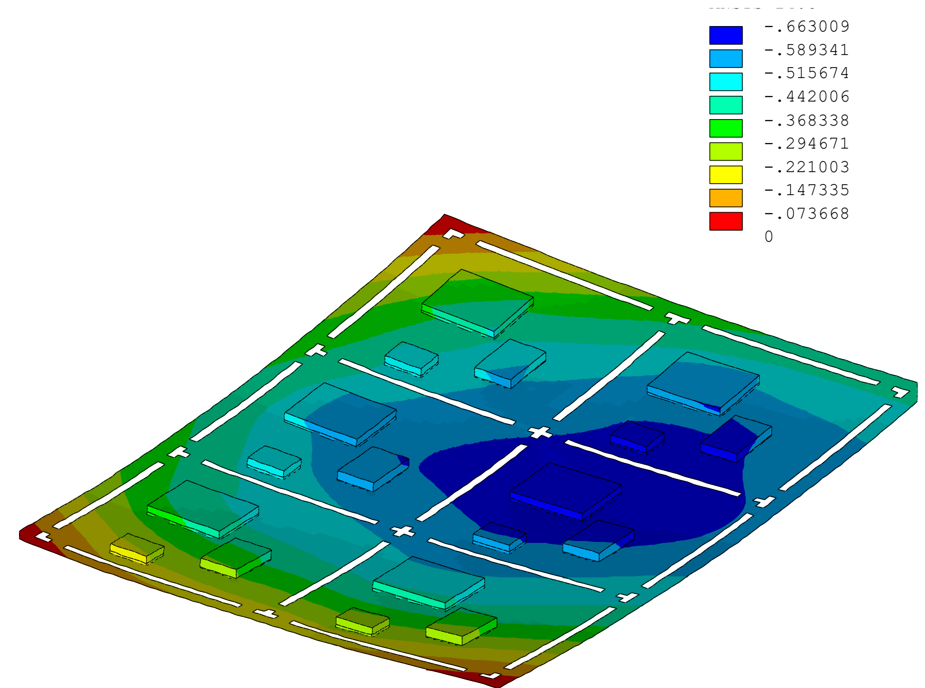







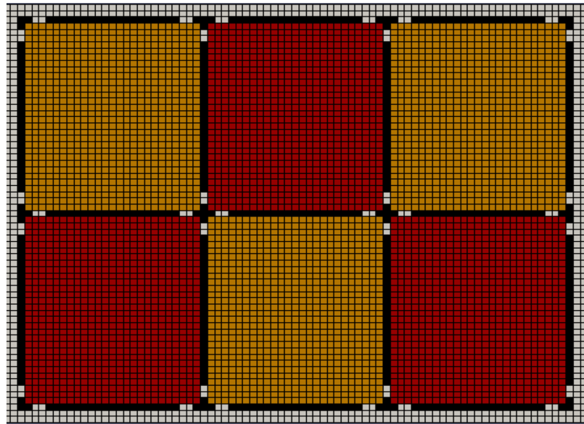
# PCBA (PCB+Chips) for SMT Process

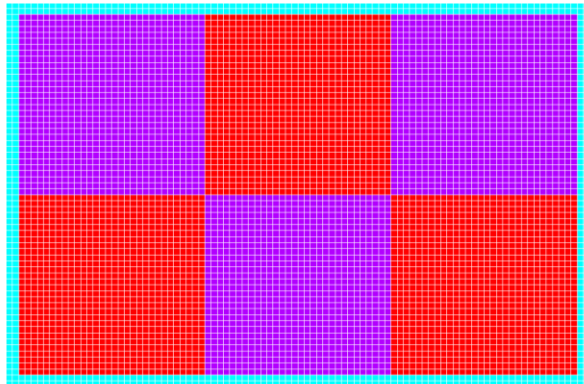




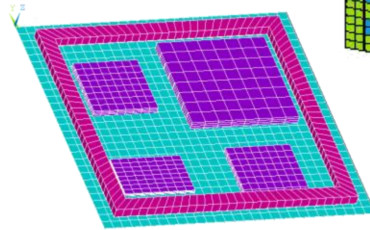
# Auto-modeling

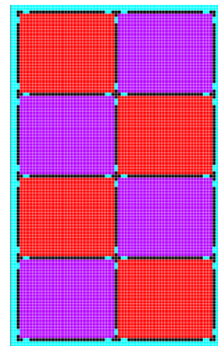
**with gap**



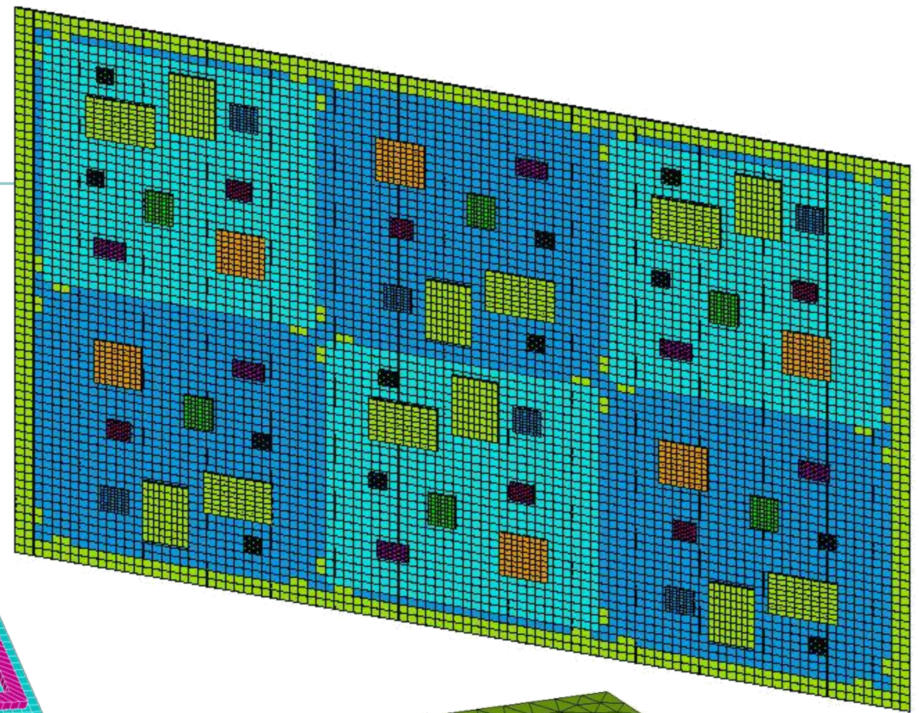


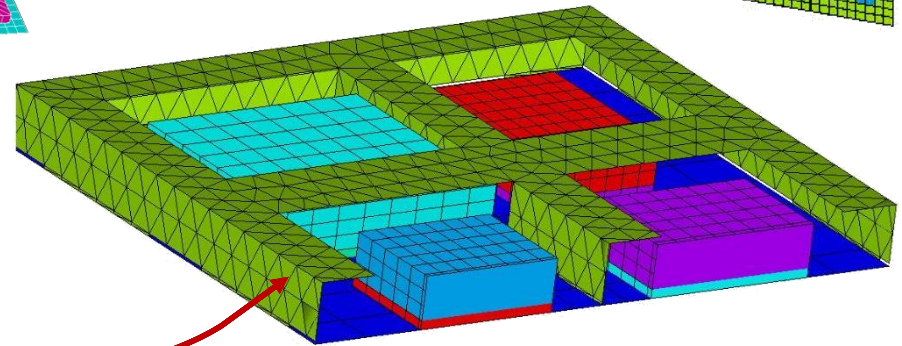
**w/o gap**

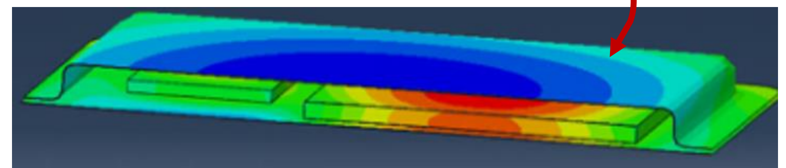




**4x2**



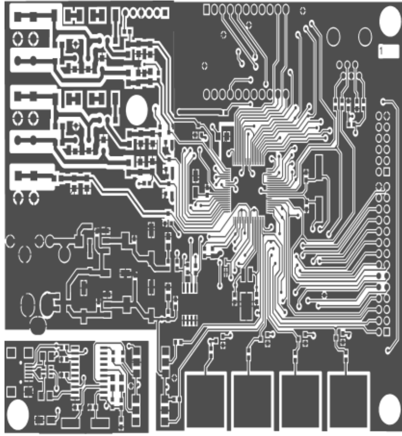


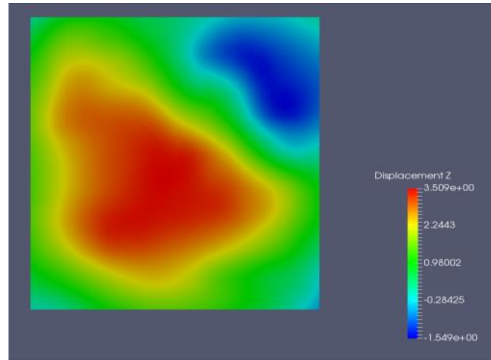


**Shielding frame**

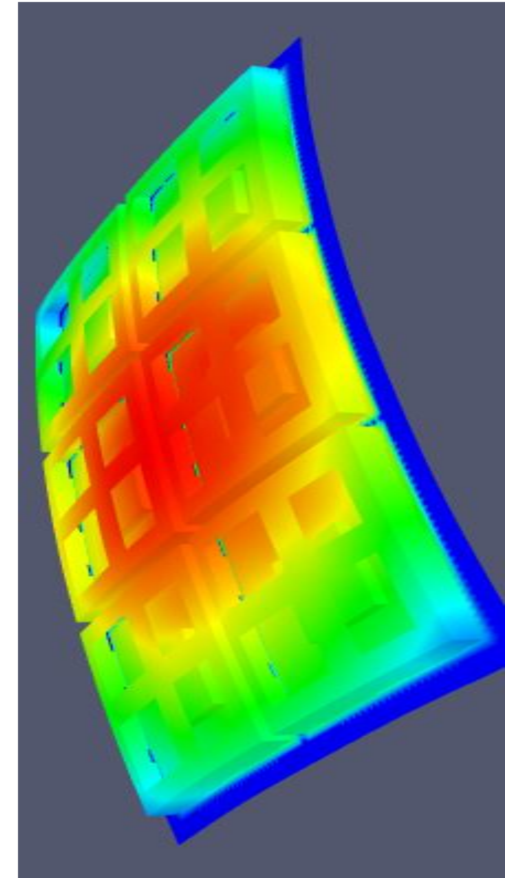
**Cap**

# PCB+PCBA Warpage:

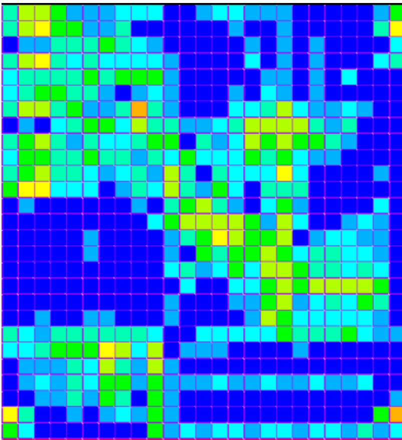


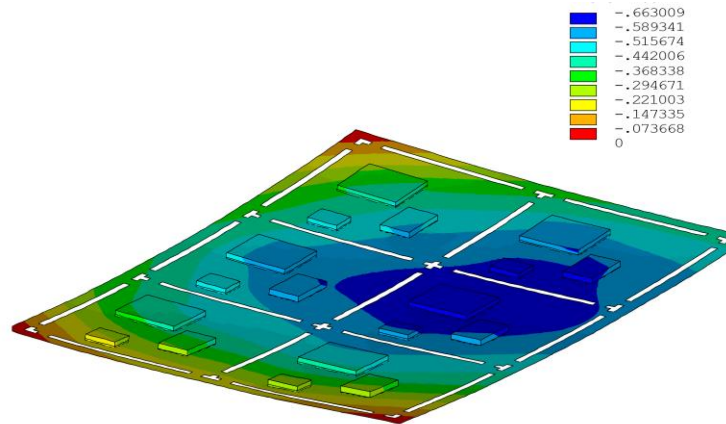



**PCB Module**



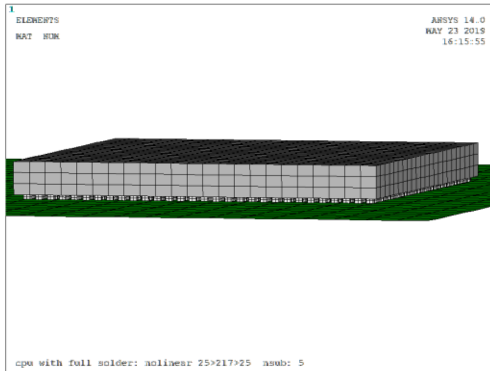
**PCBA+Frame**

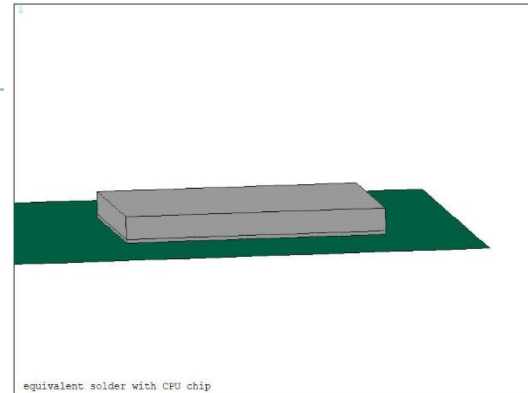


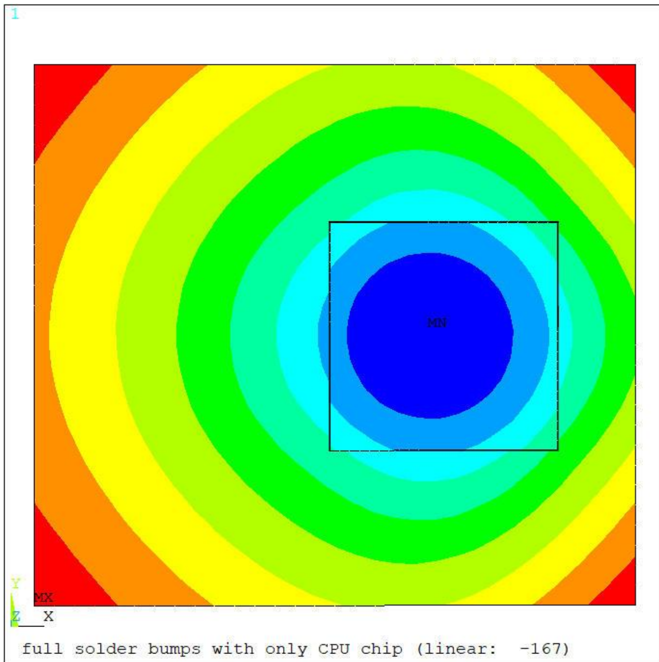


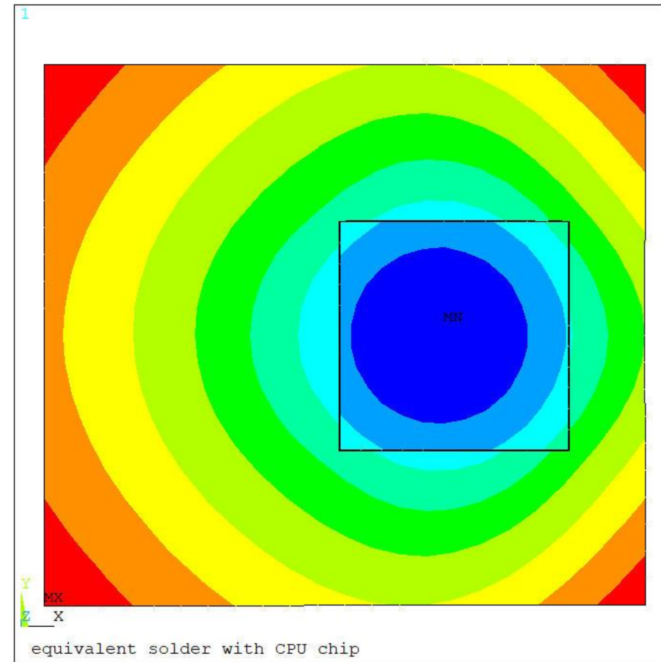

**PCBA**

**Cu Ratio**



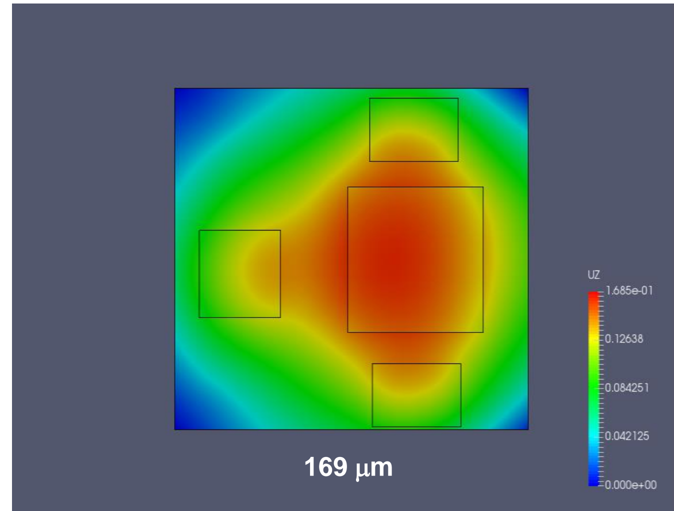




| | Full model | Equivalent model |
|---|---|---|
| Max. Displacement | 97.0 µm | 103.3 µm |

# Verification case:




| | Simulation (μm) | Experiment (μm) |
|---|---|---|
| **Maximum Warpage** | 169 | 140 |

# Web-based Simulation Platform

## Input Page

工作名稱：ting test
註解：
PCB Size：X = 60.00 mm Y = 60.00 mm
邊框(Rail)寬度：X = 4.00 mm Y = 4.00 mm
Tab：寬度 = 4.0 mm 到邊緣的距離 = 2.0 mm
進階設定：切割間隙寬度 = 2.0 mm 網格大小 = 2.0 mm
切割間隙是否挖空 是 Y 方向有無 Tab 有
銅線顏色：黑 指定鋪銅比 0.70
進階設定：Rail鋪銅 無 r1 無 Frame(2)/Stiffener(3) 3
斷面性質：Frame(Stiff.) Thick 2.000 Adhesive Thickness 0.100 Stiffener Width 3.000 KOZ 0.600
Panel 排列數量：X = 2 Y = 1
Panel 排列方式：A

**Panel layout**

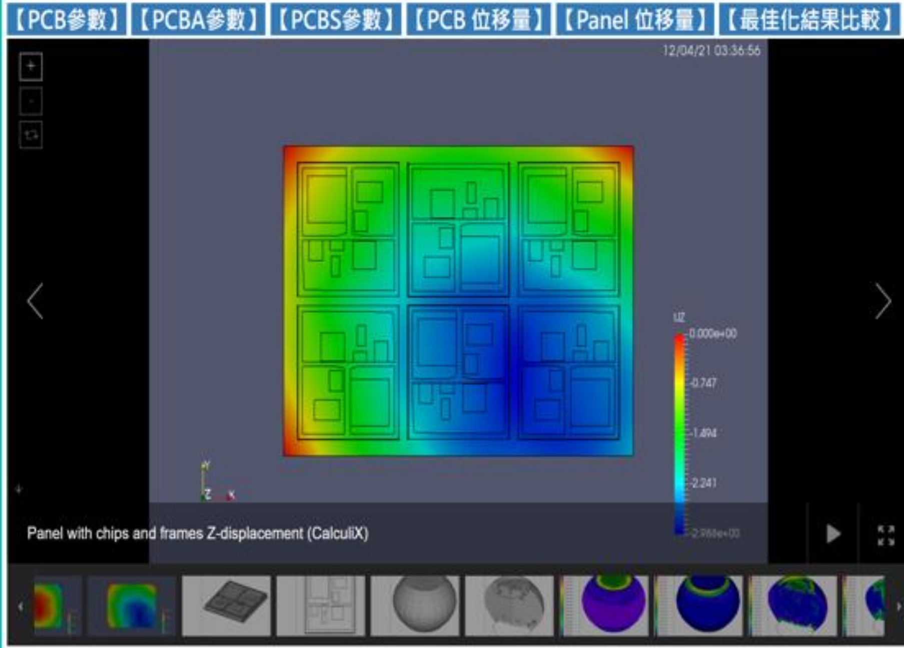
X Y A | X Y B | X Y C | (X=Y) X Y D | X Y E

綠漆層高度 20 µm 綠漆層材料 Solder_mask_default

共 10 層銅線：第 01 層銅線
銅層高度 20 µm 銅層材料 Cu_foil_default
PP層高度 20 µm PP層材料 Prepreg_default
第 02 層銅線
銅層高度 20 µm 銅層材料 Cu_foil_default
PP層高度 20 µm PP層材料 Prepreg_default

**Trace file input**

## Result Page



# Conclusions

- PCB or PCBA simulation is a multi-scaled problem
- With the proposed effective modeling method, the PCB/PCBA warpage simulation becomes feasible with a reasonable computing resources
- The simulation of the PCB/PCBA manufacturing process based on the effective modeling method becomes easy to implement